## REMARKS

Applicant thanks the Examiner for his thorough analysis of the application, and for the indication of allowable subject matter in Claims 4 and 5. For the Examiner's convenience and reference, Applicant's remarks are presented in the order in which the corresponding issues were raised in the Office Action. The distinctions identified and discussed below are presented solely by way of example to illustrate some of the differences between the claimed invention and the cited references. Applicant invites the Examiner to review any references discussed below to ensure that Applicant's understanding of the references is consistent with the Examiner's understanding.

STATUS OF THE CLAIMS

Claims 1-13 remain in the case. Claims 4 and 5 stand objected to. Claims 9-11 stand rejected under 35 U.S.C. § 101. Claims 1-3, 6-8, 12, and 13 stand rejected under 35 U.S.C. § 102(b). Claims 1, 6, 8-10, 12, and 13 have been amended. Claim 11 has been canceled. No new claims have been added.

RESPONSE TO CLAIM REJECTIONS UNDER 35 U.S.C. § 101

Claims 9-11 stand rejected under 35 USC 101 as directed to non-statutory subject matter. The Examiner argued they claim a computer program *per se*. Applicant traverses the rejection with regard to Claim 11, since it included the limitation of "a storage medium" on which the program is stored. However, that claim has been canceled, so the point with regard to Claim 11 is moot.

Claims 9 and 10 have been amended to include the limitation of "a signal bearing medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform operations to control" an information processor according to the present invention and as supported in the specification. The unamended claims already contained at least functional descriptive material, since their limitations impart functionality when employed as a computer component, i.e., causing an information processor to function as a voltage-controlling and mode-controlling module (Claim 9), or a frequency-controlling and mode-controlling module (Claim 10). MPEP 2106.IV.B.1. If the claims did not contain it already, the addition of the signal bearing medium limitation clearly gives the claims statutory subject matter as a new and useful machine. See 35 USC 101; MPEP 2106.IV.B.1 ("When functional descriptive material is recorded on some

computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized"); *In re Lowry*, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory). Applicant submits that the claims are allowable.

RESPONSE TO CLAIM REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1-3, 6-8, 12, and 13 stand rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 6,161,187 to Mason et al. (hereinafter Mason).

It is well settled that under 35 U.S.C. §102 "an invention is anticipated if . . . all the claim limitations [are] shown in a single art prior art reference. Every element of the claimed invention must be literally present, arranged as in the claim. The identical invention must be shown in as complete detail as is contained in the patent claim." *Richardson v. Suzuki Motor Co., Ltd.*, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). To be anticipated "every element of the claimed invention must be identically shown in a single reference." *In re Bond*, 910 F.2d 831, 15 USPQ 2d 1566 (Fed. Cir. 1990).

Mason teaches an apparatus and method for decreasing power consumption in a computer system by skipping and storing clock interrupts during system inactivity, presenting the interrupts to the CPU after reception of a non-interval interrupt or other event.

With regard to Claim 1, Mason does not teach or suggest the use of a low-voltage operation mode in which the system is placed before halting instruction execution. Mason decreases power consumption by remaining in a sleep, halt-instruction mode, storing interval interrupts to be dealt with after the CPU's return to normal operating voltage. As opposed to Applicants, Mason's CPU enters an execution halt mode and low-voltage mode at the same time. See, e.g., col. 8, lines 48-59.

In contrast to Mason, Claim 1 is limited to an information processor comprising a mode controlling module that places the CPU into halt mode only after a voltage controlling module has placed the CPU into a low-voltage operating mode. Mason does not teach a low-voltage operating mode (rather, only a low-voltage halt mode), nor does he teach entering a low-voltage operating mode and only then switching from instruction execution mode to execution halt mode, as claimed.

Applicant submits that the existing language in Claim 1 already indicated the difference, but Claim 1 has nonetheless been amended to make the distinction clear. See p. 13, lines 25-29 of the specification, among other portions of the specification, for support.

Applicants therefore submit that Claim 1 and its dependents are allowable over Mason.

With regard to Claim 2, in addition to the limitations in its parent claim, Mason teaches the de-assertion of a CPU_PWR_EN signal which, in its absence, stops the CPU from executing instructions "in order to place it in a low-power consuming mode." Col. 3, lines 45-48. Claim 2, in contrast, is limited to the execution and sending of a positive halt-grant instruction and signal which allows the instruction execution module to halt, this action occurring only after execution of the voltage reduction instruction. Mason does not teach the halt grant signal, nor does he teach the sequence of instruction execution claimed in Claim 2.

With regard to Claim 3, Mason teaches placing the CPU in a low-power consuming mode, storing interval interrupt assertions, with the CPU remaining in that mode until assertion of a non-interval clock interrupt or other event, at which time the CPU regains normal operating voltage and receives the stored interrupt assertions. Col. 8, line 60-col. 9, line 9.

Claim 3 is limited to the mode controlling module taking the CPU out of low-voltage halt mode and placing it in low-voltage operation mode in response to an interrupt request, only subsequently changing to normal voltage operating mode. In contrast, Mason teaches placement of the CPU directly into normal operating mode upon reception of an interrupt. Mason does remain in low-voltage mode during interval clock interrupts, but those interrupts are stored by an interface chipset, not received by the CPU as claimed in Claim 3.

With regard to Claim 6, Mason teaches placing the CPU in a low-power consuming mode in which the voltage is either zero or a value greater than zero. The Examiner maintains that the zero voltage can be considered as Applicants' Claim 6 voltage reduction mode, with the non-zero voltage being equivalent to the low-voltage operation mode. Claim 6 has been amended to make clear that the voltage reduction mode is a non-zero voltage state.

With regard to Claim 7, the Examiner maintains that Mason's non-zero reduced voltage may be viewed as the intermediate-voltage operation mode of Claim 7. With regard to Claim 7's low-voltage operation mode, however, the only statement from the Examiner is that Mason's non-zero reduced voltage can also be viewed as the low-voltage operation mode. That would make Claim 7's

intermediate-voltage operation mode the same as the low-voltage operation mode, contrary to the language of Claim 7 which plainly differentiates their voltage levels. Additionally (though the Examiner did not address this specifically) it would be impossible to view Mason's zero-voltage level as the low-voltage operation mode of Claim 7, since there must be some voltage in the low-voltage operation mode in order to enable the halting of the instruction execution module (Claim 1).

Applicant additionally notes that Mason teaches placing the CPU in *either* the zero *or* non-zero state. Col. 5, lines 50-60. Claim 7's limitations include: "said voltage controlling module operates said central processing unit and places said central processing unit into an intermediate-voltage operation mode in which the operating voltage is lower than the operating voltage in said normal mode and higher than the operating voltage in said low-voltage operation mode and *then* places said central processing unit into said low-voltage operation mode" (emphasis added), clearly limiting the claim to placing the CPU in one mode and then the other, not either one alternatively as taught by Mason.

With regard to Claim 8, Mason does teach reducing the clock frequency, as maintained by the Examiner, but (similarly to Claim 1's low-voltage mode) Mason does not teach or suggest the use of a low-frequency operation mode in which the system is placed before halting instruction execution. Mason's CPU enters an execution halt mode and low-frequency mode at the same time. See, e.g., col. 8, lines 48-59.

Similarly to Claim 1, Claim 8 is limited to an information processor comprising a mode controlling module that places the CPU into halt mode only after a frequency controlling module has placed the CPU into a low-frequency operating mode. Mason does not teach a low-frequency operating mode (rather, only a low-frequency halt mode), nor does he teach entering a low-frequency operating mode and only then switching from instruction execution mode to execution halt mode, as claimed in Claim 8. Applicant submits that the existing language of Claim 8 indicated the difference, but Claim 8 has nonetheless been amended to make the distinction clear.

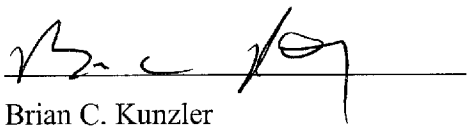
The Examiner based his rejection of Claims 12 and 13 on the statements with regard to Claims 1 and 8. Similarly, Applicant submits that amended Claims 12 and 13 are patentable for the same reasons stated above with regard to Claims 1 and 8.

ALLOWABLE SUBJECT MATTER

The Examiner indicated allowable subject matter in Claims 4 and 5, but objected to them as depending on a rejected base claim (Claims 3 and 4). Given the arguments above, Applicants submit that the base claims are also allowable.

If any impediments to the prompt allowance of the claims can be resolved by a telephone conversation, the Examiner is invited to contact the undersigned.

Respectfully submitted,



Brian C. Kunzler
Reg. No. 38,527
Attorney for Applicant

Date: July 19, 2006
8 East Broadway, Suite 600
Salt Lake City, UT 84111
Telephone (801) 994-4646 Fax (801) 531-1929

I:\Client Files\1400 Lenovo\1441-JP30051\OAR1 (ALE)\OAR1.doc